

In response to the Office Action dated June 19, 2002, please amend the above-identified application as follows:

**IN THE CLAIMS**

Please amend the claims as follows, substituting any amended claim(s) for the corresponding pending claim(s):

1. (unchanged) A CMOS integrated circuit device comprising:
  - a plurality of p-channel transistors formed in active surface areas of n-type regions, wherein the p-channel transistors do not have LDD source/drain regions;
  - a plurality of n-channel transistors formed in isolated active surface areas of p-type regions;
  - gate electrodes for the p-channel and n-channel transistors, the gate electrodes overlying and being insulated from the respective active surface areas, wherein the gate electrodes for the p-channel transistors have a width less than a minimum channel length required for the p-channel transistors;
  - p-type source and drain regions for the p-channel transistors, each p-type source and drain region consisting of a low resistivity region;
  - n-type source and drain regions for the n-channel transistors, each n-type source and drain region having a low resistivity region and an LDD region;

14           each gate electrode having a pair of sidewall spacers each having an inner and an outer  
15           portion, wherein the inner portions of the sidewall spacers for each p-channel transistor gate  
16           electrode has a width which, taken on each side of the respective gate electrode for the  
17           respective p-channel transistor and combined with the width of the respective gate electrode for  
18           the respective p-channel transistor, exceeds a minimum channel length for the respective p-  
19           channel transistor;

20           each p-channel low resistivity region located under the outer portion and at least a part  
21           of the inner portion of its respective sidewall spacer;

22           each n-channel low resistivity region located under at least a part of the outer portion and  
23           a part of the inner portion of its respective sidewall spacer; and

24           each n-channel LDD region extending from its respective low resistivity region to  
25           underlie the inner portion of its respective sidewall spacer.

1           2. (unchanged) The integrated circuit of claim 1, wherein the inner portion of the sidewall  
2           spacer comprises an oxide.

1           3. (unchanged) The integrated circuit of claim 1, wherein the inner portion of the sidewall  
2           spacer comprises an oxide.

1 4. (unchanged) The integrated circuit of claim 1, wherein the p-channel source and drain  
2 comprise silicon implanted with  $\text{BF}_2$ .

1 5. (amended) The integrated circuit of claim 1, wherein:

2 the distance between low resistivity regions of the source and drain regions of the p-  
3 channel transistor is between the p-channel minimum length and the p-channel maximum  
4 length, wherein:

5 the p-channel minimum length is a distance below which the transistor will not  
6 operate reliably due to short channel effects; and

7 the p-channel maximum length is a distance above which the transistor will not  
8 turn on efficiently.

1     6. (unchanged) The integrated circuit of claim 1, wherein:  
2             the distance between the low resistivity regions of the n-channel transistor is between  
3     the n-channel minimum LDD length and the n-channel maximum LDD length, wherein:  
4             the n-channel minimum LDD length is a distance below which the transistor will  
5     not operate reliably due to short channel effects; and  
6             the n-channel maximum LDD length is a distance above which the transistor will  
7     not turn on efficiently.

1     7. (unchanged) The integrated circuit of claim 1, wherein the sidewall spacers have a total  
2     width of approximately 500 to 2500 Å.

1 27 (amended) A CMOS integrated circuit structure, comprising:

2 an n-channel transistor including lightly doped source and drain regions within a p-type

3 region of a substrate; and

4 a p-channel transistor without lightly doped source and drain regions within an n-type

5 region of the substrate, the p-channel transistor including:

6 a gate electrode having a width less than a channel length of a channel for the p-

7 channel transistor; and

8 first and second sidewall spacers adjacent opposing sides of the gate electrode

9 and overlying a portion of the channel for the p-channel transistor and portions of source

10 and drain regions for the p-channel transistor.

1 28. (amended) A CMOS integrated circuit structure, comprising:

2 an n-channel transistor including lightly doped source and drain regions within a p-type  
3 region of a substrate; and

4 a p-channel transistor without lightly doped source and drain regions within an n-type  
5 region of the substrate, the p-channel transistor including:

6 a gate electrode having a width less than a channel length of a channel for the p-  
7 channel transistor; and

8 first sidewall spacers adjacent opposing sides of the gate electrode and overlying  
9 at least a portion of the channel for the p-channel transistor and portions of source and  
10 drain regions for the p-channel transistor,

11 wherein the width of the gate electrode is less than a minimum channel length required  
12 for the p-channel transistor.

1 29. (unchanged) The CMOS integrated circuit structure of claim 28, wherein the first sidewall  
2 spacers have a width which, taken on opposing sides of the gate electrode and combined with  
3 the width of the gate electrode, exceeds the minimum channel length required for the p-channel  
4 transistor.

1 30. (unchanged) The CMOS integrated circuit structure of claim 29, wherein the width of the  
2 first sidewall spacers, taken on opposing sides of the gate electrode and combined with the  
3 width of the gate electrode, exceeds the minimum channel length required for the p-channel  
4 transistor plus a diffusion distance for implanted dopants forming source and drain regions for  
5 the p-channel transistor.

1 31. (unchanged) The CMOS integrated circuit structure of claim 30, further comprising:  
2 second sidewall spacers adjacent the first sidewall spacers and overlying source and  
3 drain regions for the p-channel transistor.

1 32. (unchanged) The CMOS integrated circuit structure of claim 30, wherein the n-channel  
2 transistor further comprises:

3 a gate electrode having a width approximately equal to a minimum channel length  
4 required for the n-channel transistor; and

5 sidewall spacers adjacent to opposing sides of the n-channel transistor gate electrode and  
6 overlying the lightly doped source and drain regions.

1 33. (amended) An intermediate structure for use in forming a CMOS integrated circuit,  
2 comprising:

3 a p-type region for an n-channel transistor including lightly doped source and drain  
4 regions;

5 an n-type region for a p-channel transistor without lightly doped source and drain  
6 regions;

7 a gate electrode overlying a portion of the n-type region, the gate electrode having a  
8 width less than a minimum channel length required for the p-channel transistor; and

9 at least one conformal insulating layer over a top and sides of the gate electrode, the  
10 insulating layer having a thickness which, taken on opposing sides of the gate electrode and  
11 combined with the width of the gate electrode, exceeds a minimum channel length required for  
12 the p-channel transistor.

1 34. (unchanged) The intermediate structure of claim 33, wherein the insulating layer forms a  
2 mask for implanting source and drain regions for the p-channel transistor.



1 35. (unchanged) The intermediate structure of claim 34, wherein the insulating layer has a  
2 thickness which, taken on opposing sides of the gate electrode and combined with the width of  
3 the gate electrode, exceeds the minimum channel length required for the p-channel transistor  
4 plus a diffusion distance for implanted dopants forming the source and drain regions for the p-  
5 channel transistor.

1 36. (unchanged) The intermediate structure of claim 35, further comprising:  
2 source and drain regions for the p-channel transistor within the n-type region, wherein  
3 edges of the source and drain regions are spaced apart from the sides of the gate electrode.

1 37. (unchanged) The intermediate structure of claim 36, wherein the source and drain regions  
2 are low resistivity regions.

1 38. (unchanged) The intermediate structure of claim 33, further comprising:  
2 second insulating layer overlying the first insulating layer to form sidewall spacers  
3 adjacent the gate electrode upon etching of the insulating layer and the second insulating layer.

1 39. (unchanged) The intermediate structure of claim 33, further comprising:  
2 a n-channel transistor gate electrode overlying a portion of the p-type region;  
3 lightly doped source and drain regions within the p-type region aligned with the n-  
4 channel transistor gate electrode.